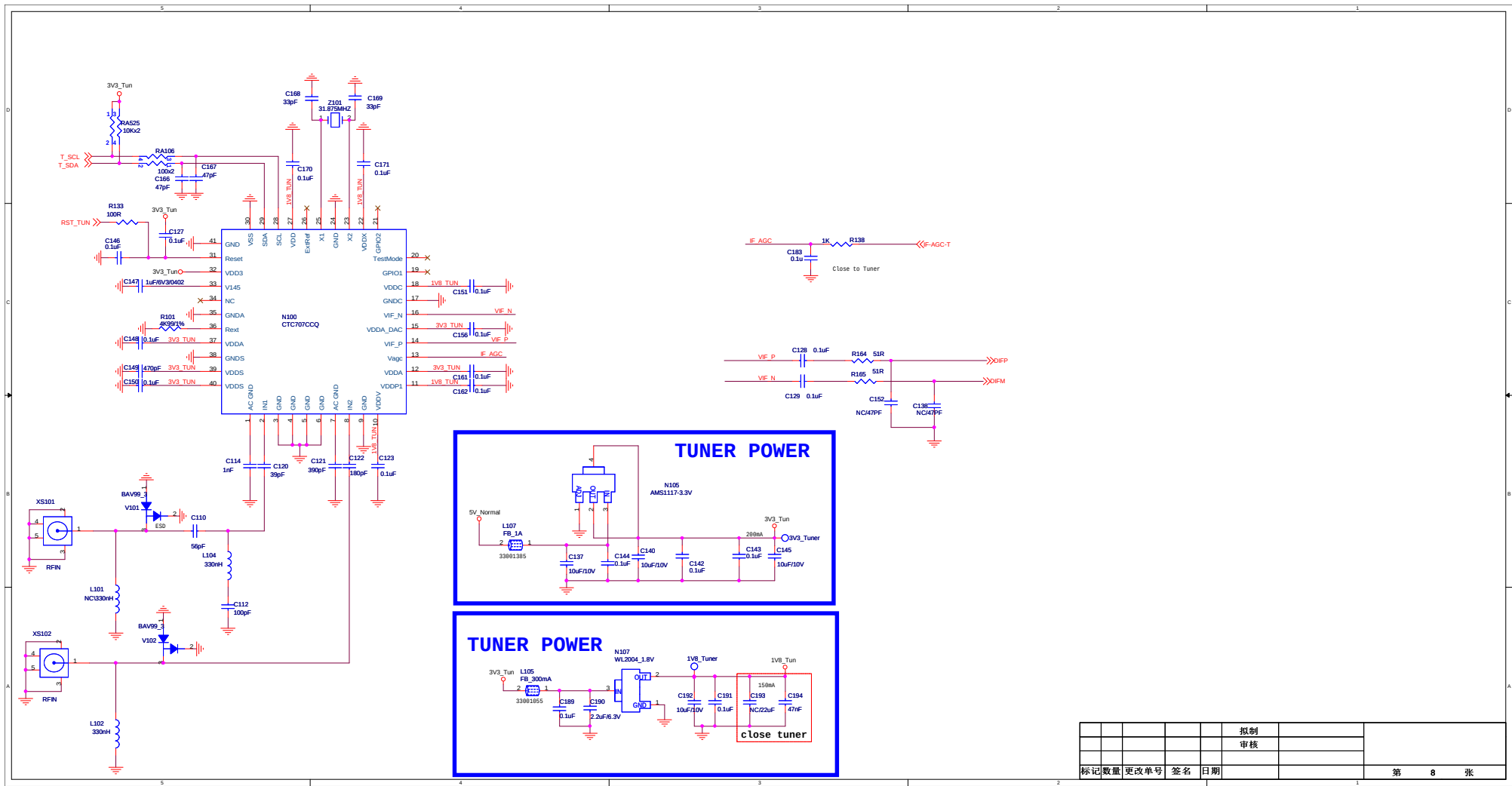




[illegible][illegible]

5V_Normal

5V_Sbs

LB10 PB_4A

33081376

R836 47k

C832 0.47uF50V

R837 47k

R838 47k

R829 100k

94C85A

V802

5V_Normal

C817 0.1uF

POWER-ON-OFF

R810 100k

V805 3904

H: On
L: Standby

Panel Power

The diagram illustrates a circuit for generating a panel power signal. It starts with a 12V VCC source connected to a 1N4001 diode (VD01) in series with a 47K resistor (RB23). The output of the diode is connected to a 0.47uF capacitor (CE27) and a 100K resistor (RB20) to ground. The other side of the capacitor is connected to the input of a 74VHC04 hex inverter (V001). The output of the inverter is connected to a 1N4148 diode (VD02) in series with a 10K resistor (RB24). The output of this second diode is connected to a 0.1uF capacitor (CE26) and a 10K resistor (RB26) to ground. The output of the second diode is labeled 'PANEL_ON/OFF'.

1.5V_DDR

5V_Nb

5V_Nb

L807 2 1

L805 2 1

NCFR-4A

FR-4A

R831 13000331

R832 13000331

R833 115/2W

115/2W

1.5V_DDR

300mA max

C813 6.1uF

C820 10uF/10V

R833 0R

C829 1V5_DDR

C813 22uF/6.3V

0.1uF

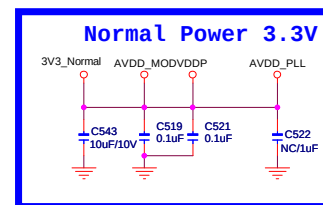
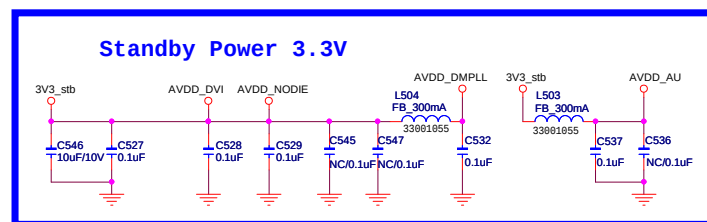
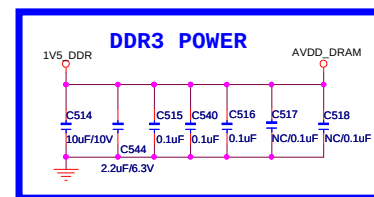
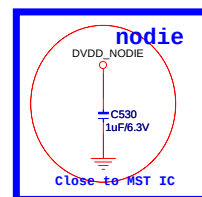
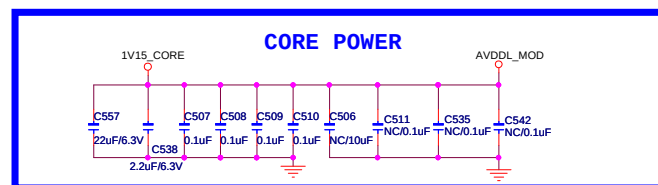
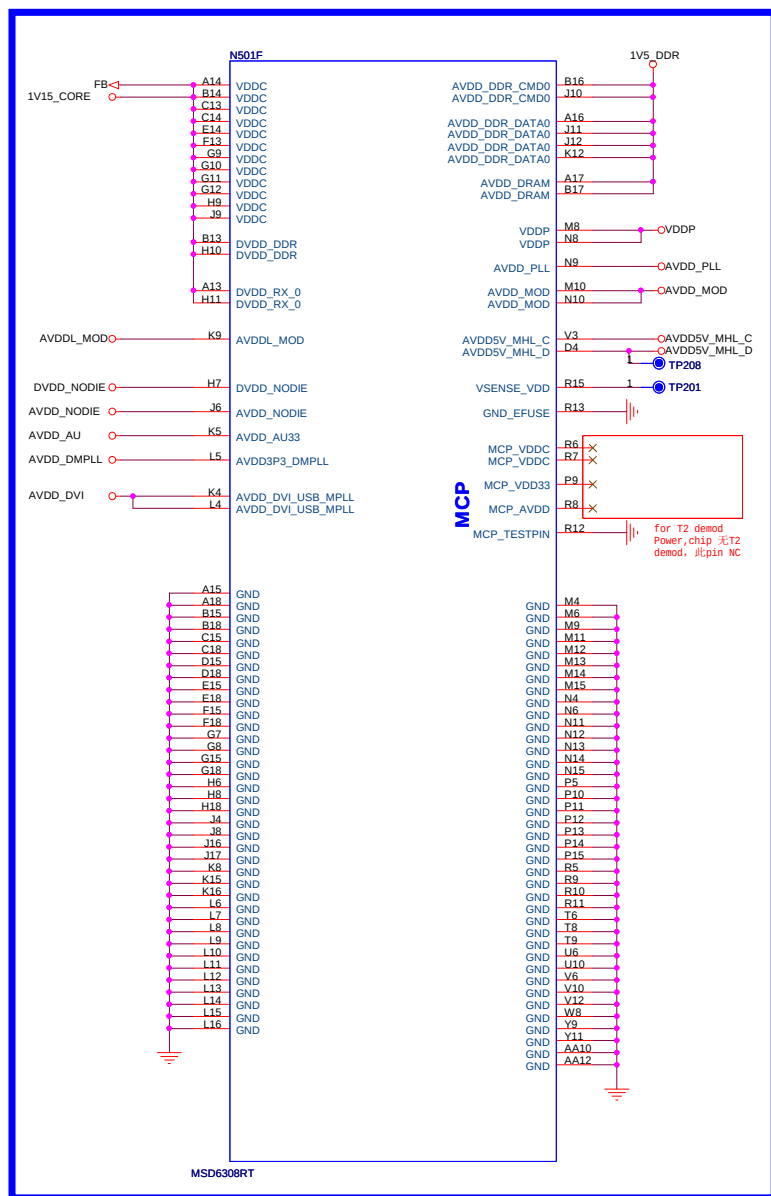
[illegible]

3.3V_normal

The diagram shows a circuit for generating a 3.3V output. It includes an LM111P timer (U1) with a timing network of a 2.2µF capacitor (C28) and a 100k resistor (R10). The output of the timer (pin 1) is connected to the base of an NPN transistor (N007, 1N4148). The emitter of the transistor is grounded, and the collector is connected to a 350mA load and a 3.3V output terminal. A 3.3V input terminal is also shown, connected to a 0.1µF capacitor (C83) to ground.

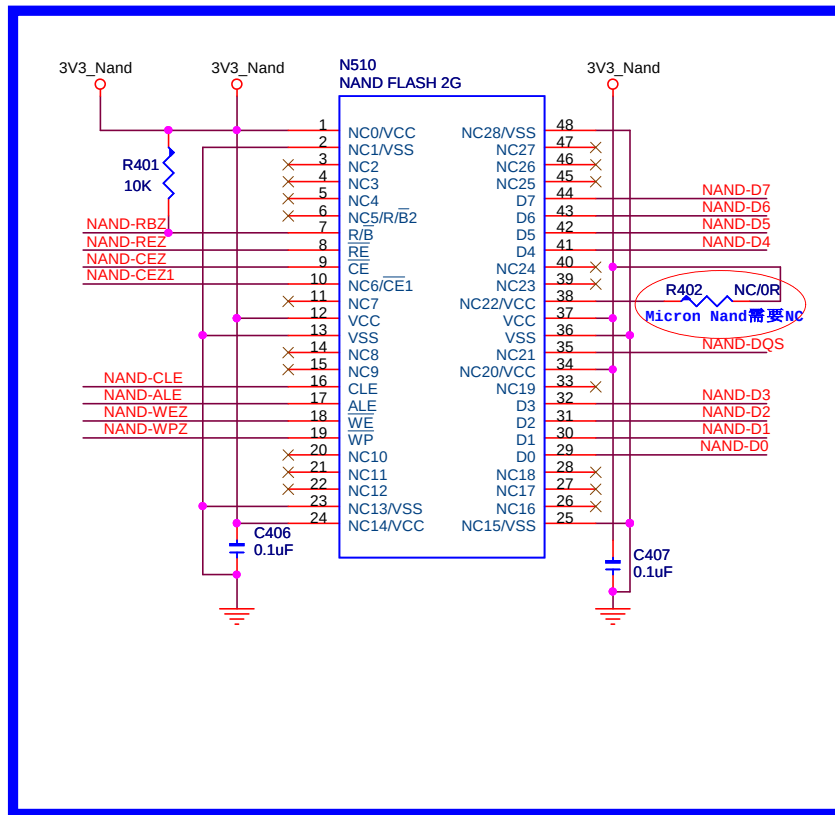
[illegible]

POWER&GND

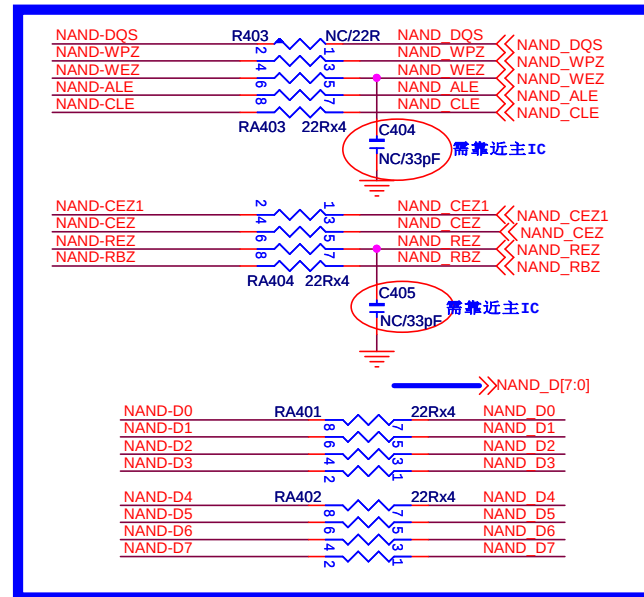
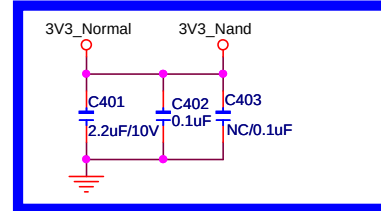


					拟制		03. MSD6308 POWER
					审核		
标记	数量	更改单号	签名	日期			第 3 张

NAND FLASH

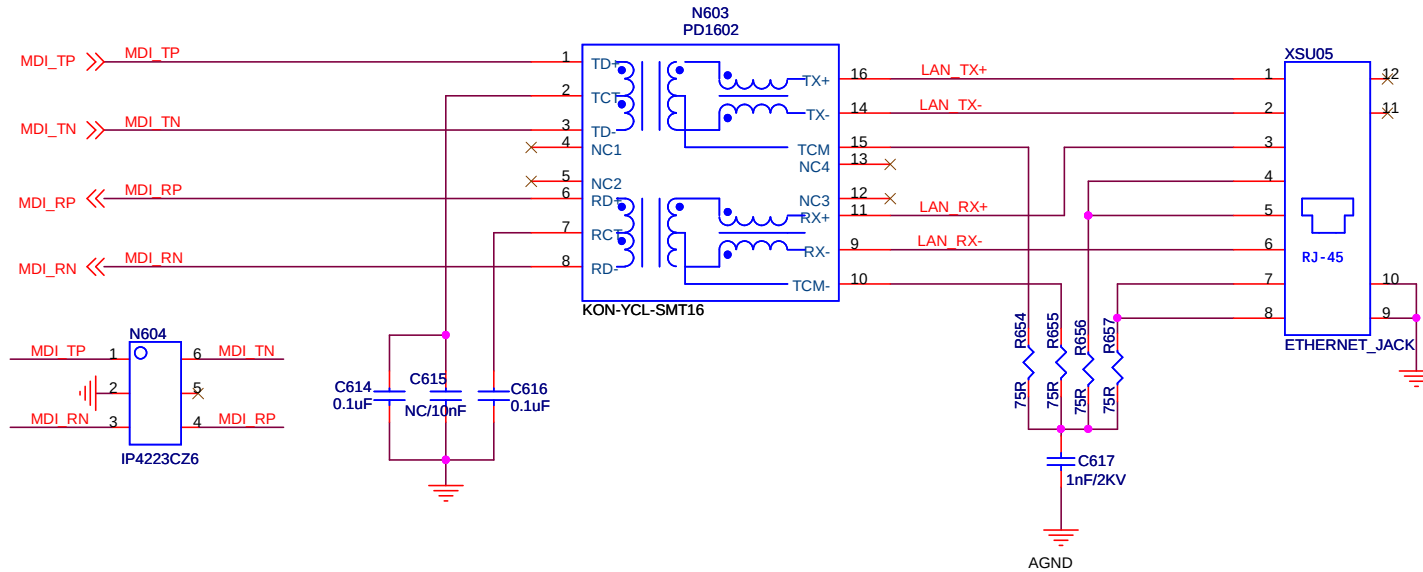


NAND Power

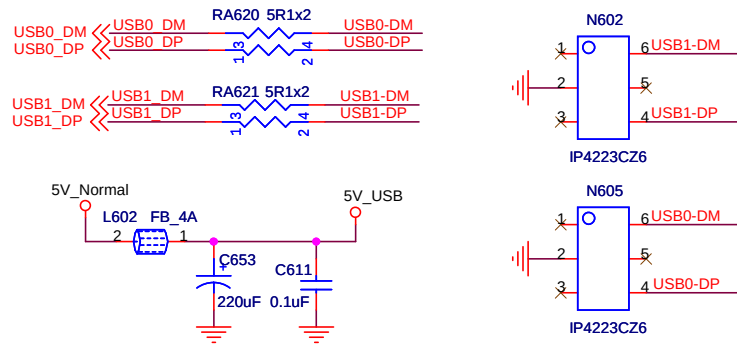


					拟制		04. NAND FLASH
					审核		
标记	数量	更改单号	签名	日期			第 4 张

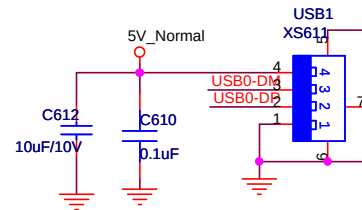
ETHERNET



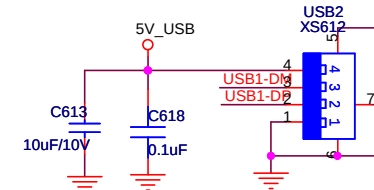
USB



内置WIFI

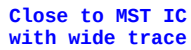


侧出



					拟制		05. ETHERNET & USB
					审核		
标记	数量	更改单号	签名	日期			第 5 张

A



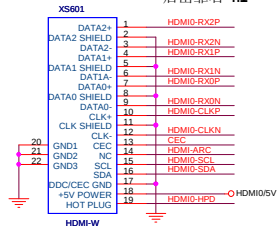
VIDEO&SPDIF OUT

The diagram illustrates the VIDEO&SPDIF OUT circuit. On the left, the XS609 connector is shown with four pins: 1 (yellow), 2 (blue), 3 (red), and 4 (black). Pin 1 is connected to AV-OUT, pin 2 to AV-OUT, pin 3 to SPDIF-OUT, and pin 4 to SPDIF-OUT. The SPDIF-OUT signal path includes a 22pF capacitor (C655) to ground, a 100R resistor (RJ08) to ground, and a 330R resistor (RJ04) to the SPDIF_OUT output. The AV-OUT signal path includes a 75R resistor (RJ26) to ground and a 0R resistor (RJ25) to the CVBS_OUT output.

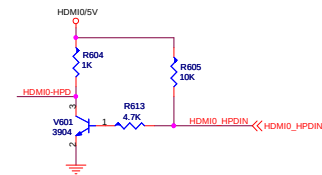
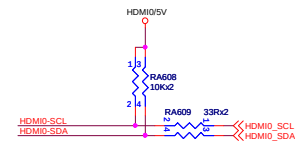
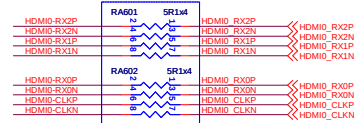
5	4	3	2	1
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HDMI1@ARC

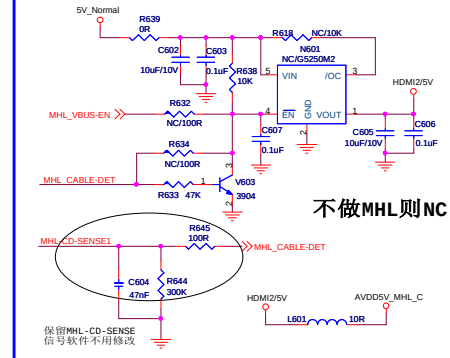
后出靠右 H1



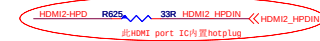
靠近端子放置



MHL for MSD6308

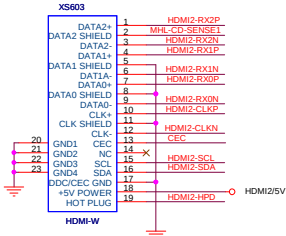


不做MHL则NC

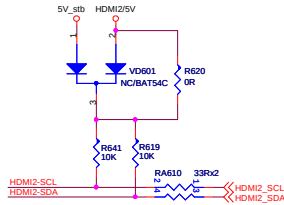
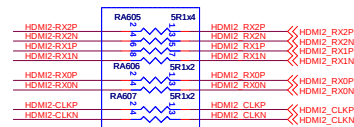


HDMI3@MHL

側出 H3

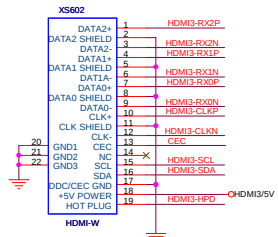


靠近IC放置

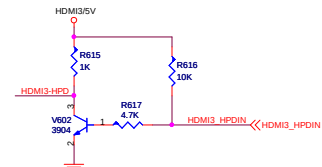
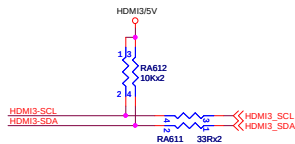
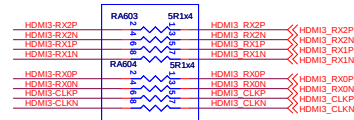


HDMI2

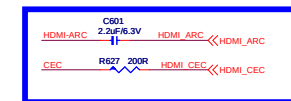
后出靠左 H2



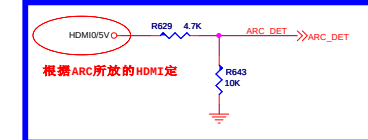
靠近IC放置



CEC & ARC



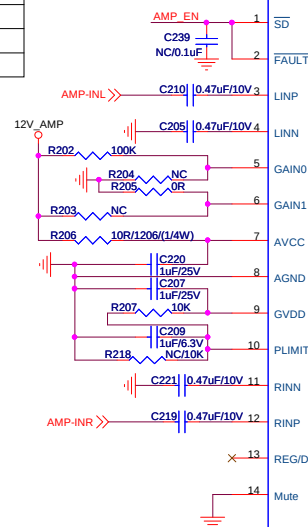
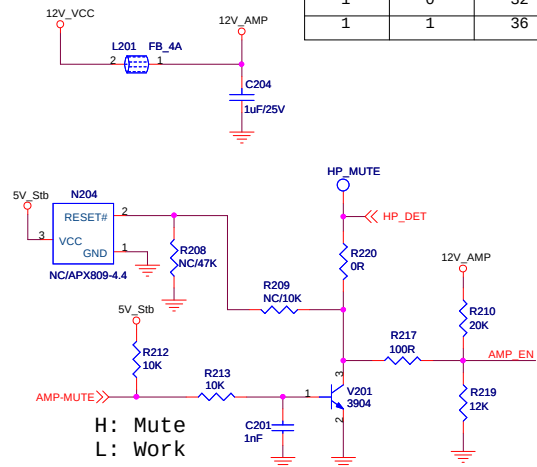
ARC DET



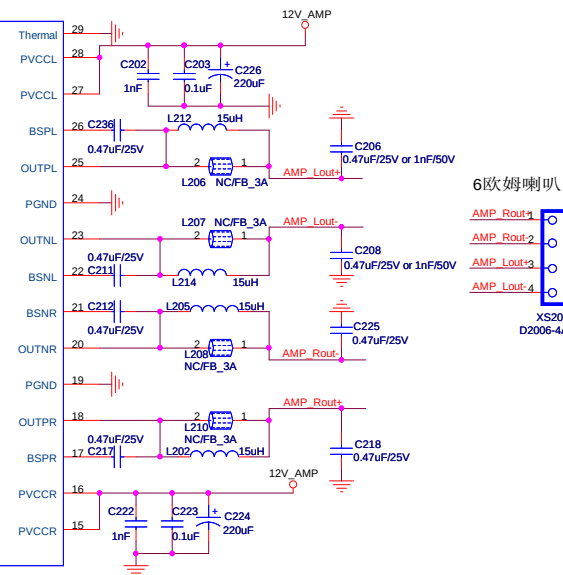
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					审核		
标记	数量	更改单号	签名	日期			第 7 张

AMP

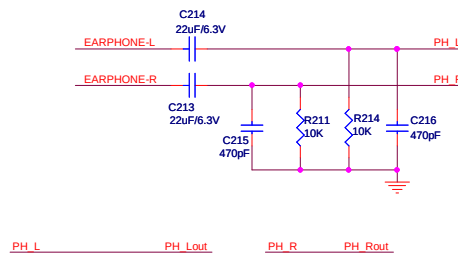
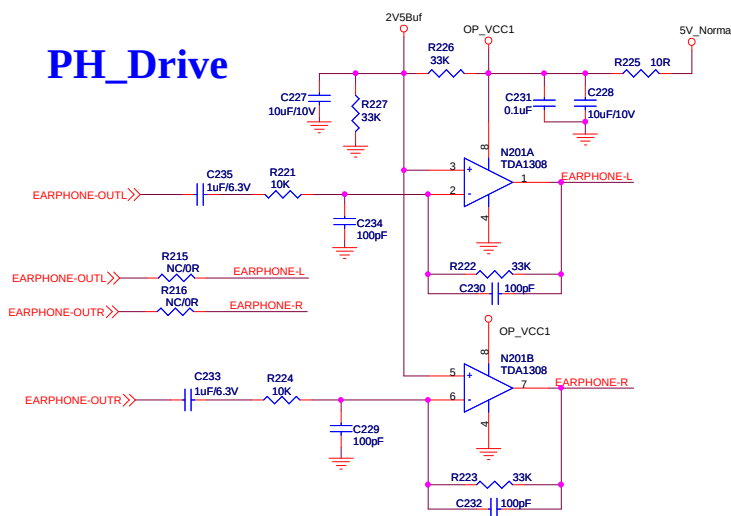
GAIN1	GAIN0	GAIN (dB)
0	0	20
0	1	26
1	0	32
1	1	36



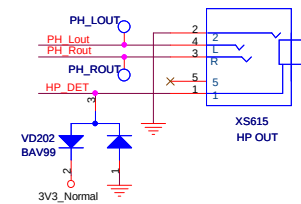
注意焊盘



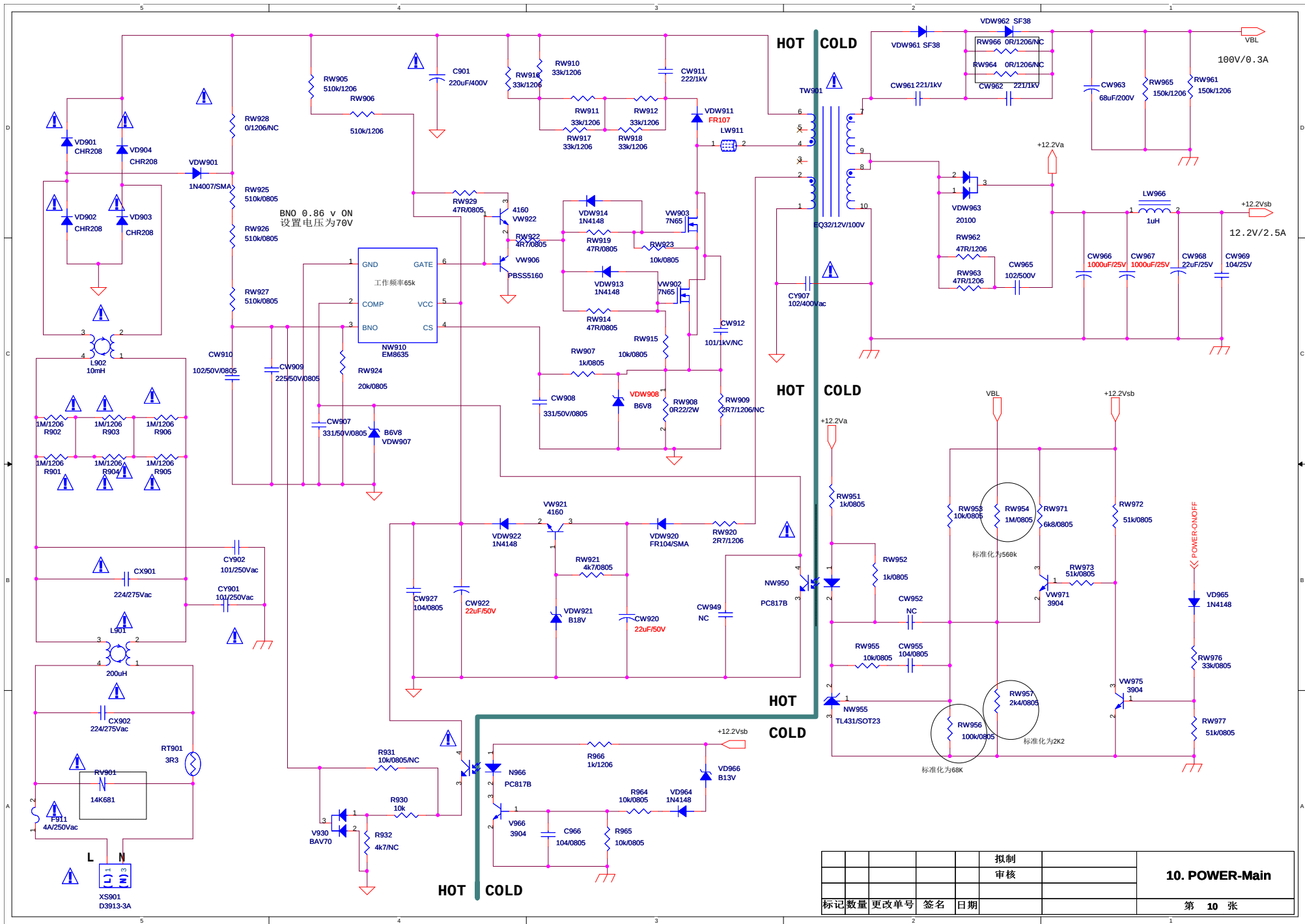
PH_Drive

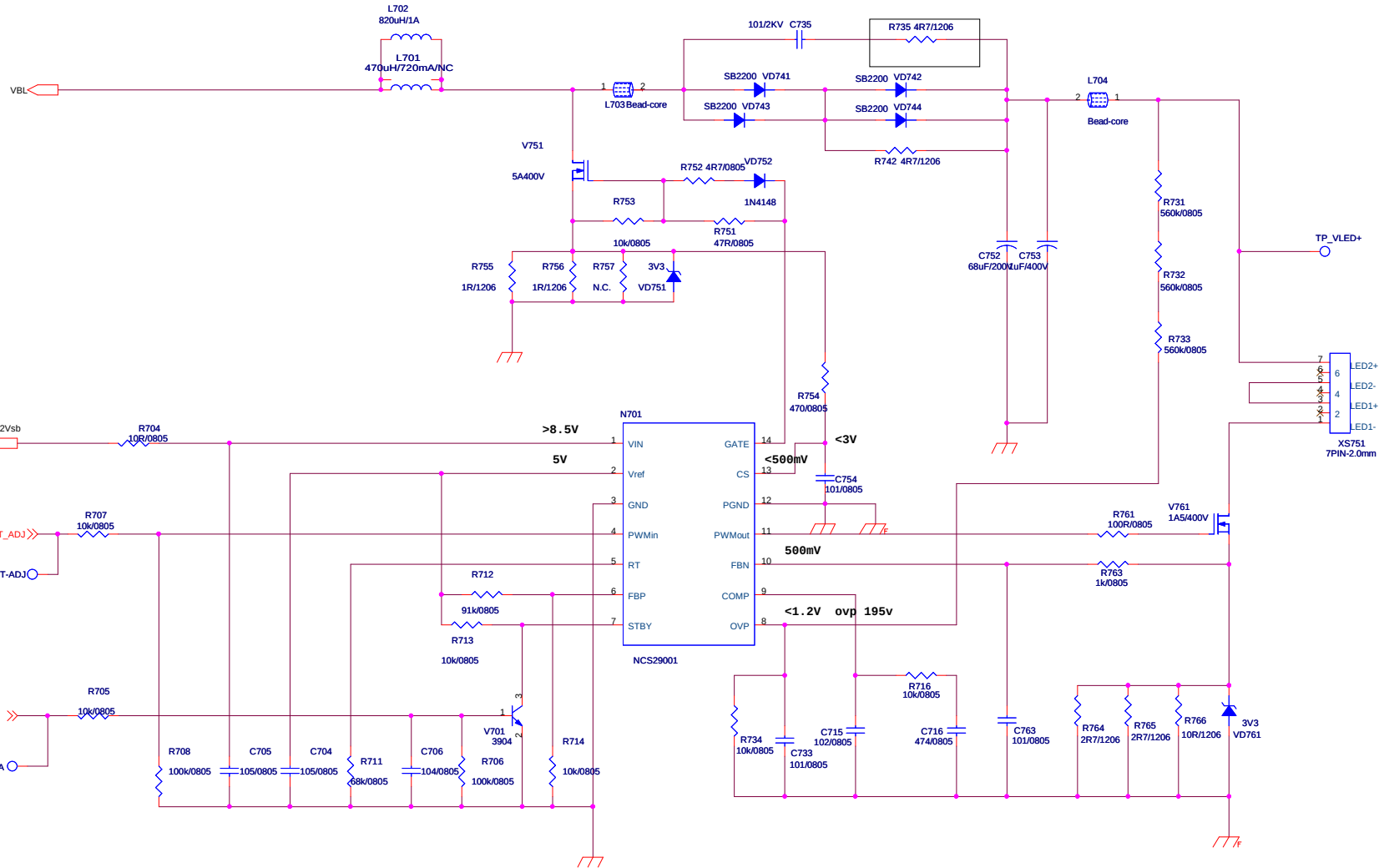


四段式耳机孔25004492
配合使用三段式耳机插头
插四段头音频线28007681



					拟制		09. Amp RT9108
					审核		
标记	数量	更改单号	签名	日期			第 9 张





$$F_o = 13750 / R_{rt} (K\Omega) = 13750 / 73 = 188 \text{ KHz}$$

$$I_{led} = 500 / R_{isen} (\Omega) = 250 \text{ mA} \quad V_{adim} > 1.5 \text{ V}$$

$$I_{led} = V_{adim} / (5 * R_{isen}) \quad V_{adim} < 1.5 \text{ V}$$

$$UVLS = 8.5 \text{ V}$$

$$OVP = 190 \text{ V}$$

						拟制		11. POWER-LED Driver
						审核		
标记	数量	更改单号	签名	日期				第 11 张